ARC430 Clock driver and DC bias board

Application Note 05 Monday, July 19, 2021

The ARC430 board contains twelve DC bias circuits with programmable output voltages from 0 to 5.0 volts. The circuits have excellent drift with temperature of 1.5 ppm per °C as well as low noise. Under load they produce 35 mA at a maximum voltage of 3.5 V. There are also twelve clocks operating between zero and a programmable voltage that has a maximum value of 4.5 volts. They each have a drive capability of 24 mA and 5 ns rise times.

Distinct voltages can be written to each of the twelve DC bias circuits and one voltage to all of the twelve clock circuits. The command to the ARM micro-controller is:

```
Arc430_writeDACData( channel, 16-bit value );
```

where ‘channel’ is 0 to 13 (13 being the clocks) and ‘value’ is a 16-bit number setting the voltage linearly over the range of zero to its maximum.

The twelve DC bias voltages are set towards the end of the “Waveforms.c” file, by the “localWaveformsInit” function. The voltages can either be set explicitly in that function or defined to a useful string. The voltages are written to the hardware after the download during system initialization.

The DC bias supplies on the ARC430 board can all be turned on or off without disturbing their programmed value with the ARM micro-controller commands:

```
Arc430_enableDCBiases ( true );     // to turn on
Arc430_enableDCBiases ( false );    // to turn off
```

In G4 the voltages can be changed in the ARC-430 control window or with the manual commands:

```
‘RWDC’   channel number (0 to 12)   16-bit value   // To write to the DAC
‘RWDC’   channel number (0 to 12)                  // To read DC bias circuit
                                                   //   voltage and current
```

The first argument returned when reading is the voltage in floating point volts, and the second argument is the current in floating point mA. Note that the DC bias circuits are all identical but the circuit for reading the currents is configured with lower gains for channels 0 to 5, meant for loads that require higher currents than channels 6 to 11. Channel 12 is the clock driver voltage. There is a loop for measuring these voltages and currents that is executed from the FPGA in much the same what that the board temperature loop operates. In G4 the loop is enabled and disabled in the ARC-430 window or with the manual commands:

```
‘EDBL’   1   // To enable the DC bias reading loop
‘EDBL’   0   // To disable the DC bias reading loop
```

There are two SMA connectors near the center of the front of the board. They may be used to transmit high speed clocks over coaxial cables in high speed, phase sensitive applications. Their driving circuit is of the same design as the remaining clocks, but they each have separate drivers. Any one of the 12

clocks can be selected for outputting on each of these two connectors with the two ARM micro-controller commands:

Arc430_HighSpeedClock5(address , enable [1] or disable [0]); for CON5
Arc430_HighSpeedClock6(address , enable [1] or disable [0]); for CON6

“address” selects which of the twelve clocks [0 to 11] is selected. Note that CON6 is located to the right of CON5.

Near the backplane connector is a grid of though holes below labels in silk screen. These are test points for measuring power supply voltages. The clock driver board was chosen to have these since it is normally the topmost board, so the power supply voltages will suffer the most ohmic losses over the backplane. Some of the values are zero and reserved for future use, and the -6V is an error. The values below are nominal values in volts.

AV	+36V	zero	VDD	3.3V	3.30 volts
AV	+16V	zero	VDD	2.5V	2.60 volts
AV	+6V	5.5 volts	VDD	1.8V	1.8 volts
AV	-16V	zero	DGND		Digital Ground
AGND		Analog Ground	AV	-6V	-2.8 volts